EE/CprE/SE 492 Weekly Report 6
3/13/25 - 4/17/25
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members
Calvin Smith – Accelerator Design lead
Camden Fergen – DevOps and Project Lead
John – Testing Lead
Nicholas – Harden and Verification lead
Levi – Communication Interfaces Lead

Weekly Summary
We worked on FGPA testing until we accidentally crashed our computer that was linked to the FPGAs, our primary benchmark was hardcoded to ensure that it will run as a standalone on the FPGA for testing by implementing memcpy() from string.h. CyGRA 2.0 is in the works and Verilog testbenches are becoming more robust, and we gained knowledge with the logic analyzers.

Pask Week Accomplishments

- Calvin:
    - Laid out FFT mappings for the CyGRA
    - Defined our kernel for FFT
    - Began writing CyGRA 2.0 with register files for processing elements
    - Refactored CyGRA code for future compatibility and potential extension
- Camden:
    - Learned how the current version of the CyGRA works as it's been a while since I last was involved with it/discussed it
    - Wrote a test bench for the PE_ARRAY in the CyGRA to ensure I understood what I was doing
    - Semi-ported the CICD pipeline to the CyGRA
- John:
    - Working on the CyGRA and implemented FFT
    - Working on the benchmarks
    - Working with Verilator to test that our verilog will correctly compute dot product

- Levi:
    - Working on the benchmarks
- Nicholas:
    - Figured out how to flash caravel project onto fpga.
    - Changed design so SRAM gets set to do sequential reads/writes.
    - Learned how to look at logic analyzers.
    - Worked on trying to flash firmware onto FPGA.

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	• CyGRA • CyDMA • CyFFT • CyRegFiles	10	130.044
Camden	• Understanding of new CyGRA • Simple test bench for PE_ARRAY to show understanding	10	120
John	• FFT Implemented • Benchmarks and Verilator	15	145
Levi	• Worked with John to create baseline mathmult-int test	7	113
Nicholas	• SRAM configuration • FPGA testing	10	146

<u>Plans for Upcoming Week</u>

- Calvin:
    - Hopefully finish up CyGRA 2.0 for integration with the testing
- Camden:
    - Now that I understand the CyGRA, write test bench for decoder + CyGRA (should be fairly simple)

    - Hardcode CICD pipeline for CyGRA Verilog files (just to make it work)
- John:
    - Hopefully be able to properly test our code with simulator
    - Make sure that CyGRA is almost completed and that we are able to test soon
- Levi:
    - Work with nick and John for testing
- Nicholas:
    - Finally run firmware on design

Summary of weekly advisor meeting

Met with Dr Duwe and gave an update about our current progress on the project. He was happy with our progress but does want us to ensure we get our FPGA testing completed to have a real "product" since we no longer will be getting the chip fabricated. Beyond that he shared some good news that there is a chance we will get the chip from last semester back, but unlikely we will see it personally.